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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,386	11/14/2003	Andrew H. Barr	200308581-1	3950

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EXAMINER	
BHAT, ADITYA S	
ART UNIT	**PAPER NUMBER**
2863	

DATE MAILED: 03/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/714,386	BARR ET AL.	
	Examiner	Art Unit	
	Aditya S. Bhat	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/14/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Jenkins et al. (USPN 6,002,868).

With regards to claim 1, Jenkins et al. (USPN 6,002,868) teaches a computer system comprising:

a processor; (100 figure 1)

a memory controller coupled to the processor; (104 figure 1)

a memory coupled to the memory controller; (108 figure 1)

a first input/output (I/0) controller coupled to the memory controller; (136;figure 1)

a first expansion slot coupled to the first I/0 controller; and (138; figure 1)

a test module card coupled to the first expansion slot; (Col.1, lines 31-32)

wherein the test module is configured to cause tests to be performed on the memory using direct memory access (DMA). (Col. 3, lines 55-57)

With regards to claims 2 and 16, Jenkins et al. (USPN 6,002,868) teaches an operating system, wherein the processor is configured to cause the operating system to be booted, and wherein the test module card is configured to cause the tests to be

performed on the memory using the first bus subsequent to the operating system being booted. (Col.4, lines 24-34)

With regards to claims 3 and 17, Jenkins et al. (USPN 6,002,868) teaches an operating system, wherein the processor is configured to cause the operating system to be executed, and wherein the test module card is configured to cause the tests to be performed on the memory using the first bus during execution of the operating system. (Col.4, lines 24-34)

With regards to claim 4, Jenkins et al. (USPN 6,002,868) teaches a second I/0 controller coupled to the memory controller; a second expansion slot coupled to the second I/0 controller; and an I/0 device coupled to the second expansion slot. (114,118;figure 1)

With regards to claim 5, Jenkins et al. (USPN 6,002,868) teaches the test module card is configured to cause tests to be performed on the memory by providing read and write transactions to the first I/0 controller. (638;figure 6c)

With regards to claim 6, Jenkins et al. (USPN 6,002,868) teaches the read and write transactions comprise DMA transactions. (Col. 3,lines 56)

With regards to claim 7, Jenkins et al. (USPN 6,002,868) teaches a bus bridge coupled to the processor and the first I/0 controller. (110;figure1)

With regards to claim 8, Jenkins et al. (USPN 6,002,868) teaches a system controller that comprises the memory controller. (104; figure 1)

With regards to claim 9, Jenkins et al. (USPN 6,002,868) teaches a method performed by a test module card coupled to an input/output (I/0) controller in a computer

system that includes a memory comprising: selecting a portion of the memory for testing during operation of the computer system; (Col.1, lines 28-31)

generating a test transaction; (308,310; figure 3) and

providing the test transaction to the portion using direct memory access (DMA). (Col. 3, lines 55-57)

With regards to claim 10, Jenkins et al. (USPN 6,002,868) teaches detecting an error that occurs in response to the test transaction; and performing a remedial action in response to detecting the error. (Col. 8, lines 26-40)

With regards to claim 11, Jenkins et al. (USPN 6,002,868) teaches providing the test transaction from the test module to the I/0 controller;

providing the test transaction from the I/0 controller to a bus bridge; (Col.3-4, lines 53-67 & 1-2)

providing the test transaction from the bus bridge to a system bus; (Col.3, lines 44-45)

providing the test transaction from the system bus to a memory controller; (Col. 3, lines 28-29) and

providing the test transaction from the memory controller to the portion.(104,108; figure 1)

With regards to claim 12, Jenkins et al. (USPN 6,002,868) teaches storing information in the memory in response to the test transaction being a write transaction. (516;figure 5b)

With regards to claim 13, Jenkins et al. (USPN 6,002,868) teaches in response to the test transaction being a read transaction: (516;figure 5b)

providing information associated with the test transaction from the portion to the memory controller; (see figure 1)

providing the information from the memory controller to the system bus; (see figure 1)

providing the information from the system bus to the bus bridge; (see figure 1)

providing the information from the bus bridge to the I/0 controller; (see figure 1) and

providing the information from the I/0 controller to the test module. (see figure 1)

With regards to claim 14, Jenkins et al. (USPN 6,002,868) teaches providing the test transaction from the test module to the I/0 controller; (Col.9, lines 28-39)

providing the test transaction from the I/0 controller to a system controller; (Col.9, lines 28-39)

providing the test transaction from the system controller to a memory controller; (Col.9, lines 28-39) and

providing the test transaction from the memory controller to the portion. (Col.9, lines 28-39)

With regards to claim 15, Jenkins et al. (USPN 6,002,868) teaches a computer system comprising:

a processor;(100;figure 1)

a memory controller coupled to the processor and configured to perform error correction (104 figure 1)

a memory coupled to the memory controller; (108 figure 1)

an input/output (I/0) controller coupled to the memory controller; (136;figure 1)

an expansion slot coupled to the I/0 controller; (138; figure 1) and

a test module card coupled to the expansion slot; (Col.1, lines 31-32)

wherein the test module is configured to cause tests to be performed on the memory by providing read transactions associated with the memory to the I/0 controller. (Col. 7,lines 45-55)

With regards to claim 18, Jenkins et al. (USPN 6,002,868) teaches the bus comprises a system bus. (102;Col. 3,line 29)

With regards to claim 19, Jenkins et al. (USPN 6,002,868) teaches the test module is configured to cause tests to be performed on the memory using direct memory access (DMA). (Col. 3, lines 55-57)

With regards to claim 20, Jenkins et al. (USPN 6,002,868) teaches direct memory access (DMA) transactions. (Col. 3, lines 55-57)

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Schieve (USPN 5,423,029) teaches a circuit and method for

testing direct memory access, Cheung (USPUB 2004/0216018) teaches direct memory access controller and method, Jewett (USPN 6,263,452) teaches a fault tolerant computer system with online recovery and reintegration of redundant components, Adler (USPUB 2003023703) teaches a method for electronically testing memory modules.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aditya S Bhat whose telephone number is 571-272-2270. The examiner can normally be reached on M-F 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on 571-272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BRYAN BUI
PRIMARY EXAMINER

Aditya Bhat
February 25, 2005